REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the Application. Dependent Claims 3, 10 and 17 have been amended for reasons of dependency. Independent Claims 1, 8 and 15 have been amended, and Claims 21-23 are new. Accordingly, Claims 1, 3-8, 10-15, and 17-23 are currently pending in the Application.

I. Rejection of Claims 1, 3-8, 10-15 and 17-20 under 35 U.S.C. § 103

The Examiner has rejected Claims 1, 3-8, 10-15 and 17-20 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. 2002/0085578 A1 to Dell, *et al.* ("Dell") in view of U.S. patent No. 6,667,983 B1 to Lo, *et al.* ("Lo") and U.S. Patent No. 6,963,576 to Lee ("Lee") in the Examiner's Action mailed August 3, 2007. The Applicants responded in an Amendment of October 15, 2007. The Advisory Action of November 5, 2007 did not enter the previous amendments, and also presented further arguments by the Examiner.

Amended Claim 1 is directed to a head blockage avoidance system. The system includes a priority summarizer configured to generate a priority summary of the packets within the m inputs and the n packet FIFOs. The n packet FIFOs occupy a same hierarchical level. The priority summarizer indicates which of the n packet FIFOs *that is to receive* a highest priority packet from one of the m inputs. The head avoidance blockage system further comprises a scheduler configured to cause packets in the n packet FIFOs to be queued for processing based on the priority summary such that packets in a packet FIFO *that is to receive* said highest priority packets are triggered to be processed *before* packets in other of said n packet FIFOs. (Emphasis added.)

As discussed in the previous Amendment of May 21, 2007, Dell is directed to a switching

stage that employs crossbar devices. (*See* page 2, paragraph [0013].) In Dell, the "switch fabric of the present invention is a cell-switching engine handling fixed-sized switching cells." (*See* page 6, paragraph [0090].) Dell uses one or more crossbars to achieve scalability in self-routing of cells. (*See* page 2, paragraph [0012].)

As was also discussed in the previous Amendment of May 21, 2007, Lo is directed to a scalable arbiter for arbitrating between multiple FIFO entry points of a network interface card. (*See* Abstract.) Lee is directed toward an arbitration scheme that is used for scheduling connections between input ports and output ports.

The Examiner cites Dell for the proposition that:

> Dell at al further discloses summarizing priority of packets from FIFOs, indicating which of the packets contains or is to receive a highest priority, and scheduling the packets for processing based on the summarized priority such that packets in a packet FIFO that contain the highest priority are triggered to be processed before packets in other FIFOs (See page 8, paragraph 107 and page 10 paragraphs 145-153 of Dell et al. for reference to an arbiter receiving bids summarizing packet priority from packets of the FIFOs and for reference to arbitrating between packets based on priority such that packets in a FIFO *that contain the highest priority are* ***always*** *processed* ***before*** *packets in other FIFOs*). (*See* Examiner's Action, page 3; emphasis added.)

In Claim 1, however, the priority summarizer prioritizes for an n packet FIFO ***that is to receive*** *a highest priority packet...* such that packets in a packet FIFO that *is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs,* which is not disclosed or suggested in Dell. (Emphasis added.)

However, unlike the invention of Claim 1, Dell arbitrates between packets based on priority such that packets in a FIFO *that* ***contain*** *the highest priority are* ***always processed before*** *packets in other FIFOs.* (*See* Examiner's Action, page 3; emphasis added.)

In the present Application, in one embodiment of Claim 1:

> [0044] ... [A]dditionally, the head of line blockage avoidance system 300 includes a scheduler 360. The scheduler 360 is configured to cause one of the packet FIFOs 330, 332, 340, 342 to be queued for processing based on the priority summary.
>
> [0046] *In order to prevent head of line blockage of the packet having a high priority in the first source FIFO 310 by the packet having a low priority in the first packet FIFO 330,* ***the scheduler 360 would queue the first [low priority] packet FIFO 330 to be processed first.*** (Emphasis added.)

In other words, in one embodiment of Claim 1, as determined from the priority summary, the scheduler 360 schedules a lower priority packet within an n packet FIFO ***before*** a higher level priority packet within an n packet FIFO... such that packets in a packet FIFO that contains or is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs.

In one embodiment of Claim 1:

> [0044] This [*i.e.,* the scheduler 360] would queue the first (low priority) packet FIFO 330 to be processed first] would allow the packet having the low priority in the first packet FIFO 330 to be transferred to the destination FIFO 336. Then, the packet having a high priority would be transmitted toward the first packet FIFO 330 and the first packet FIFO 330 would be processed next. *Thus, the head of line blockage is avoided.* (Emphasis added.)

In the Advisory Action, the Examiner states that:

> In response to Applicant's argument that Dell et al. discloses always processing packets in a FIFO that contains the highest priority before packets in other FIFOs and thus is different from the claimed invention, the Examiner respectfully disagrees. First, it is pointed out that the priority arbitration disclosed by Dell et al. whereby high priority class arbitration always overrides low priority class arbitration is only a single embodiment and not essential to the invention of Dell et al. (See Advisory Action, page 2.)

The Applicants respectfully state that the argument made by the Applicants has been misconstrued by the Examiner. The above example was cited from Dell et al. by the Examiner as

anticipating elements of the present invention of Claim 1. The Applicants therefore analyze the cited passages of Dell to illustrate that the cited passages do *not* contain elements of presently amended Claim 1, that of a priority summarizer that prioritizes for an n packet FIFO ***that is to receive*** *a highest priority packet...* such that packets in a packet FIFO ***that is to receive*** said highest priority packets are triggered to be processed before packets in other of said n packet FIFO. The Applicants respectfully submit that the cited reference teaches away from Claim 1.

The Examiner states:

> Next, although the Applicant points out that the specification of the present Application discloses a situation where a lower priority packet is transferred to a destination before a higher priority packet, this argument is moot, since there is no claim limitation necessitating this situation. The independent claims merely contains limitations to "scheduling packets ... based on said priority summary..." and there is no limitation requiring a lower priority packet to be scheduled before a higher priority packet. (*See* Advisory Action, pages 2-3.)

The Applicants respectfully state that the Examiner has mischaracterized the arguments made the Applicants and the cited claim language as previously presented, and does not apply to Claim 1 as currently amended. Claim 1 reads as follows: "a priority summarizer configured to generate a priority summary of said packets within said m inputs and said n packet FIFOs that indicates which of said n packet FIFOs *is to receive a highest priority packet* from one of said m inputs... such that packets in a packet FIFO that *is to receive* said highest priority packets are triggered to be processed *before* packets in other of said n packet FIFOs." (Emphasis added.) The Applicants respectfully state that the Examiner has not yet addressed the language of *is to receive* a highest priority packet; nor the language of such that packets in a packet FIFO that *is to receive said* highest priority packets are triggered to be processed before packets in other of said n packet FIFOs."

Furthermore, the Applicants are unable to find within Dell a teaching or suggestion of a priority summarizer configured to generate a priority summary of said packets within said m inputs and said n packet FIFOs that indicates which of said n packet FIFOs packet FIFOs *is to receive a highest priority packet* from one of said m inputs" as is claimed in Claim 1.

Also, the Examiner states "there is no limitation requiring a lower priority packet to be scheduled before a higher priority packet." (See Examiner's Action, page 3.)

The Applicants respectfully cite language of Claim 1, as clarified and amended: "a scheduler configured to cause packets in said n packet FIFOs to be queued for processing based on said priority summary ... *such that packets in a packet FIFO that is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs.*" (Emphasis added). The Applicants respectfully request that the Examiner withdraw the argument.

Furthermore, the Applicants respectfully state that the argument is not moot. This is because the argument illustrates one example of a consequence of an embodiment of the invention of amended and clarified Claim 1, which the Applicants respectfully state is not disclosed or suggested in Dell.

The Examiner contends that Lo discloses the newly added claim elements. The Examiner states:

> Lo et al discloses using a different transmit FIFO entry point circuit 410-416 for each different transmission priority level (See column 9 lines 31-33 of Lo et al.). Since all packets having the highest priority go to the transmit FIFO entry point circuit having corresponding to the highest priority, the pointer used by Lo et al. to sort packets corresponding to the highest priority transmit FIFO entry point circuit inherently also corresponds to the transmit FIFO entry point circuit that is to received a highest priority packet. Thus, Lo et al disclose this claim limitation. (*See* Advisory Action page 3.)

Lo states: "Circuit 405 of FIG. 7 provides a separate transmit FIFO entry point circuit 410-416 for each different transmission priority level ("type").

The Applicants respectfully disagree with the Examiner's characterization of Claim 1 as applied to the cited reference. In Lo, each entry point 410-416 of Lo has a fixed priority, which is then arbitrated by the scalable priority arbiter 420. However, Claim 1 recites: "a priority summarizer configured to generate a priority summary of said packets within said m inputs and said n packet FIFOs that indicates *which* of said n packet FIFOs *is to receive a highest priority packet* from one of said m inputs." (Emphasis added.) In Lo, however, the entry point 410-416, and therefore the inputs of the scaleable priority arbiter 420, have *constant* priorities. Therefore, Lo does not disclose or suggest "a priority summarizer configured to generate a priority summary of said packets within said m inputs and said n packet FIFOs that indicates *which* of said n packet FIFOs is to receive a highest priority packet from one of said inputs".

Furthermore, with the newly added dependent Claims 21-23, it is apparent, under the Doctrine of Claim Differentiation, that the priority summarizer of these claims is configured to be able to generate a priority summary.... that indicates which of said n packet FIFOs are capable of *both* containing or receiving a highest priority packet. Claims 21-23 contain elements of the previously presented independent Claims 1, 8 and 15, respectively.

Nor has the Examiner cited Lee as curing the deficiencies of Dell or Lo regarding a priority summarizer as claimed in Claim 1. Therefore, the Examiner has not presented a *prima facie* case of rejection of Claim 1. In view of the foregoing remarks, the cited references do not support of the Examiner's rejection of independent Claim 1, nor for similar reasons the rejection of independent Claim 8 and Claim 15, nor their dependent claims, when considered as a whole. Therefore, Claims

3-8, 10-15, and 17-20 are nonobvious over the cited references under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection of Claims 1, 3-8, 10-15, and 17-20 and allow issuance thereof.

II. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this Application to be in condition for allowance and therefore earnestly solicit s a Notice of Allowance for Claims 1, 3-8, 10-15, and 17-23. Furthermore, the Applicant reserves the right to address arguments and positions in the Examiner's Action at a later date that are not addressed in the present Amendment.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present Application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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